high-speed clock oscillator; LOCO low-speed clock oscillator; TR**1** to TR**12**, TR**21** to TR**25**, TR**31**, TR**40** MOS transistor

**1**. A data processing device comprising:

a load circuit including a central processing unit and operated by supplied electric power;

a step-down power supply circuit stepping down an external power supply voltage and including an output node coupled to the load circuit, the step-down power supply circuit including:

a first step-down unit stepping down the external power supply voltage, and

a bias current control circuit controlling a magnitude of bias current flowing through an auxiliary path from the output node to a ground, the auxiliary path is separate from a path to the load circuit; and

a control circuit increasing the magnitude of the bias current, prior to a change of an operation state of the load circuit by which a relatively large change occurs to an amount of current consumed by the load circuit,

wherein the bias current control circuit includes a first MOSFET (Metal-Oxide Semiconductor Field-Effect Transistor) having a source-drain path as the auxiliary path and a gate coupled to receive a first bias control signal from the control unit,

wherein when the load circuit makes a transition from a state of relatively high power consumption to a state of relatively low power consumption, the control circuit increases the magnitude of the bias current, prior to the transition, by outputting the first level of the first bias control signal to the gate of the first MOSFET to turn on the first MOSFET, and

wherein after a predetermined time from the transition, the control circuit decreases the magnitude of the bias current by outputting a second level of the first bias control signal to the gate of the first MOSFET to turn off the first MOSFET.

**2**. The data processing device according to claim **1**,

wherein the transition is a first transition,

wherein when the load circuit makes a second transition from a state of relatively low power consumption to a state of relatively high power consumption, the control circuit increases the magnitude of the bias current, prior to the second transition, by outputting the first level of the first bias control signal to the gate of the first MOSFET to turn on the first MOSFET, and

wherein after a predetermined time from the second transition, the control circuit decreases the magnitude of the bias current by outputting a second level of the first bias control signal to the gate of the first MOSFET to turn off the first MOSFET.

**3**. The data processing device according to claim **1**, further comprising:

wherein the first step-down unit includes:

a differential operational amplifier amplifying a potential difference between a reference voltage and the output node;

an output transistor provided between the output node and an external power supply node and including a gate connected to an output of the differential operational amplifier; and

a second MOSFET having a source-drain path coupled between the output node and the ground and having a gate coupled to receive a second bias control signal from the control unit,

wherein the control circuit

provides a first level of the second bias control signal in the whole period of the state of relatively high power consumption as well as a starting period and an ending period of the state of relatively low power consumption to turn on the second MOSFET, and

provides a second level of the second bias control signal except for the starting and ending periods of the state of relatively low power consumption to turn off the second MOSFET.

**4**. The data processing device according to claim **3**, further comprising:

wherein the bias current control circuit further includes a third MOSFET having a source-drain path coupled in series to the source-drain path of the first MOSFET and having a gate coupled to receive the second bias control signal,

wherein the third MOSFET turns on by the first level of the second bias control signal and turns off the second level of the second bias control signal.

**5**. The data processing device according to claim **3**, further comprising:

wherein the bias current control circuit further includes a third MOSFET having a source-drain path coupled in series to the source-drain path of the first MOSFET and a gate coupled to the output node.

**6**. The data processing device according to claim **1**,

wherein the load circuit includes a component operating at least in the state of relatively low power consumption,

wherein the step-down power supply circuit further includes a second step-down unit stepping down the external power supply voltage,

wherein the first step-down unit operates only in the state of relatively high power consumption, and

wherein the second step-down unit operates in the state of relatively high power consumption and the state of relatively low power consumption.

**7**. The data processing device according to claim **3**, further comprising:

wherein a current control by the control circuit is according to the first transition.

**8**. The data processing device according to claim **1**, further comprising:

wherein the central processing unit includes a processor, and the first step-down unit includes a first step-down circuit.

**9**. A data processing system comprising:

a battery;

a sensor unit;

a timer unit;

a communication unit; and

a data processing device operated by a power supply voltage supplied from the battery, boosted at a predetermined time interval by the timer to make a first transition from a state of relatively low power consumption to a state of relatively high power consumption in response to an output of the timer unit and to perform a processing on output signals from the sensor, outputting the processed data to the communication